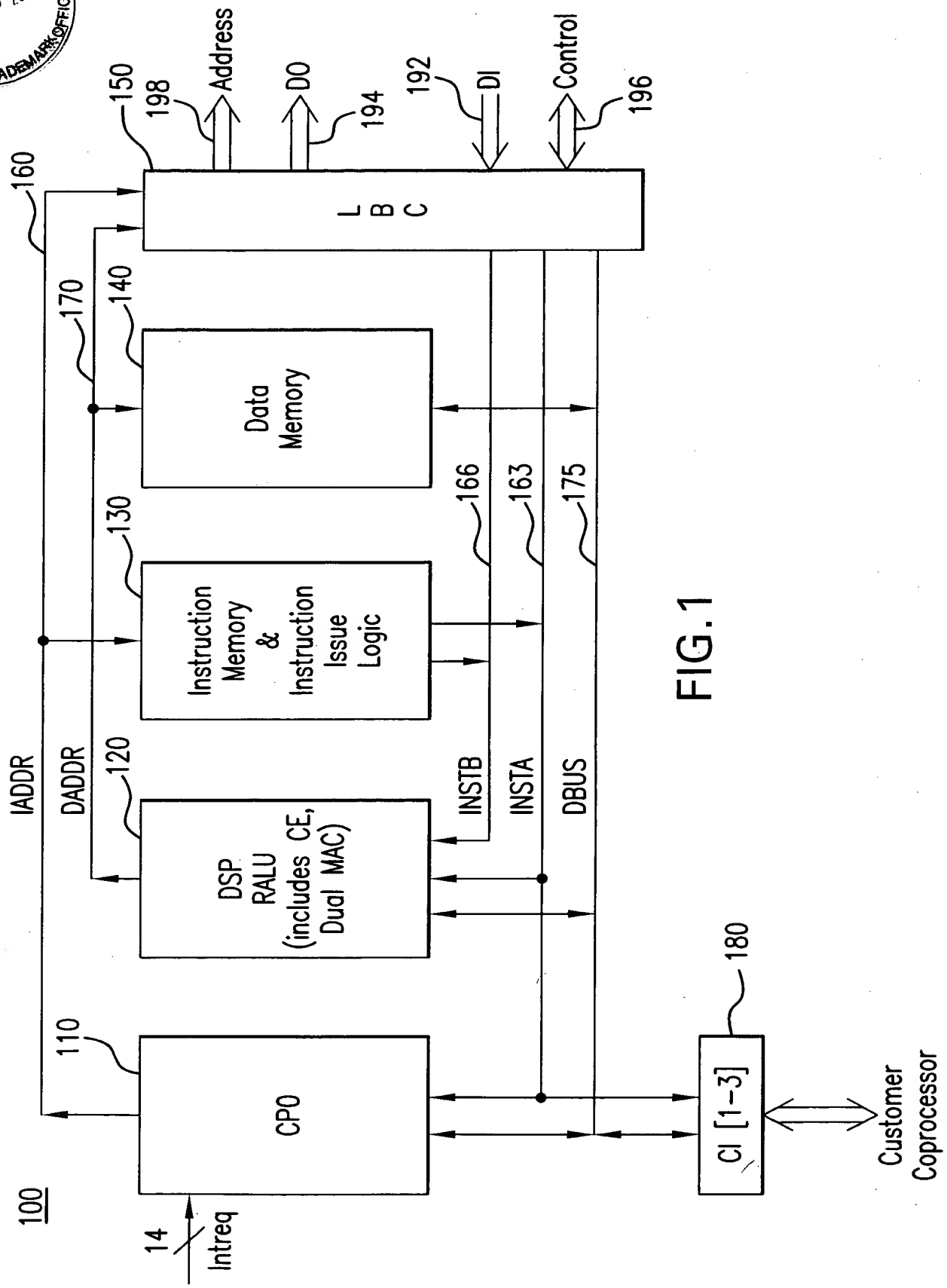


FIG. 1

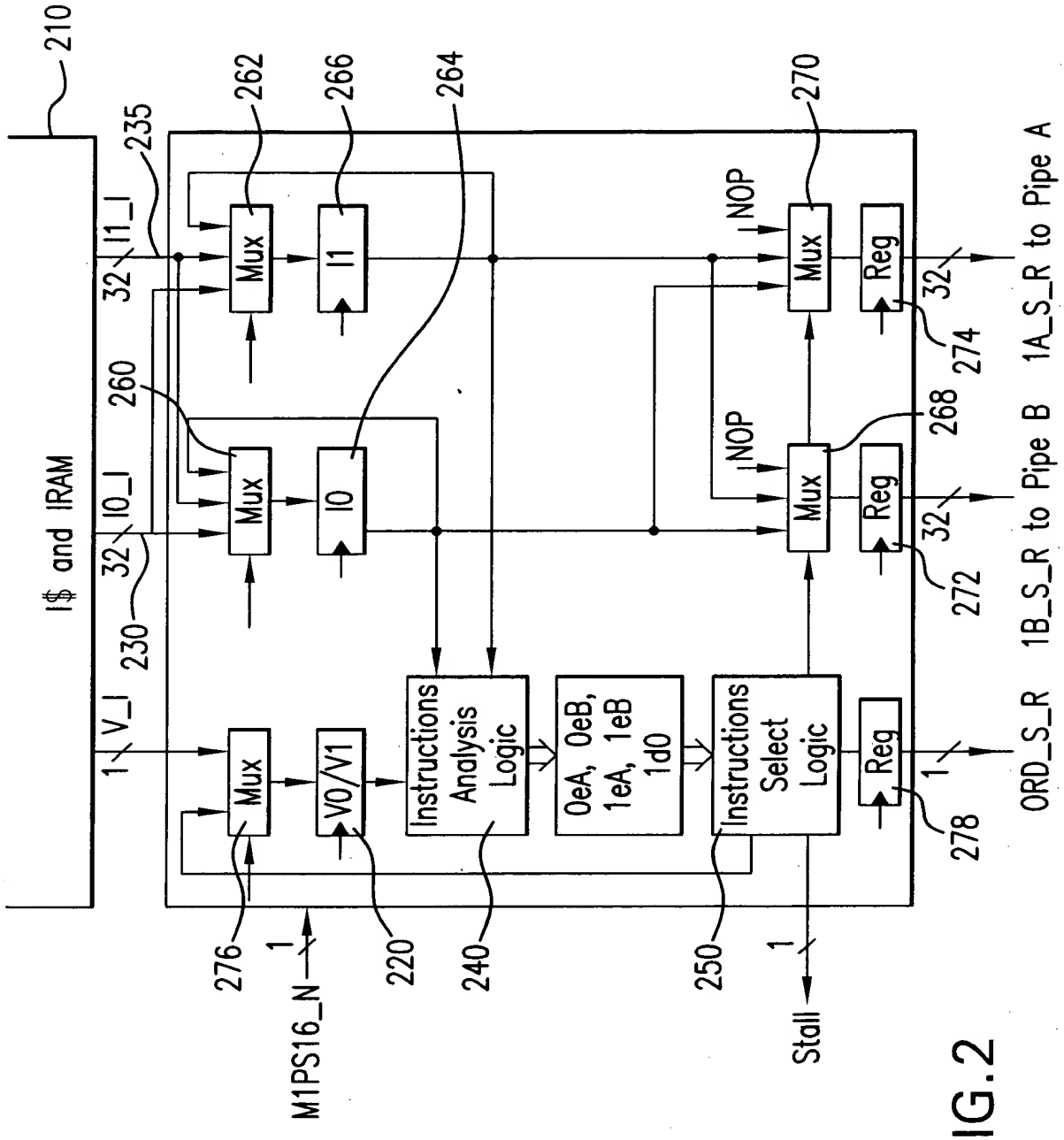

210
I$ and IRAM
235
I1_I
32
262
Mux
I1
266
264
270
NOP
Mux
Reg
32
274
260
I0_I
32
230
Mux
I0
NOP
Mux
268
Reg
32
272
V_I
1
Mux
V0/V1
Instructions Analysis Logic
0eA, 0eB, 1eA, 1eB 1d0
Instructions Select Logic
Reg
1
278
276
1
M1PS16_N
220
240
250
1
Stall
1A_S_R to Pipe A
1B_S_R to Pipe B
ORD_S_R

FIG.2

INSTRUCTION SELECT LOGIC

300

		0eA : 0eB			
		00 (I0 NOT VALID)	01	11	10
1eA:1eB	00 (I1 NOT VALID)	IA ← NOP IB ← NOP ORD ← d/c V[1:0] ← NEXT	NOT POSSIBLE	NOT POSSIBLE	NOT POSSIBLE
	01	IA ← NOP IB ← 11 ORD ← B V[1:0] ← NEXT	IA ← NOP IB ← 10 STALL ← 1 ORD ← B V[1:0] ← 01	IA ← 10 IB ← 11 ORD ← A V[1:0] ← NEXT	IA ← 10 IB ← 11 ORD ← A V[1:0] ← NEXT
	11	IA ← NOP IB ← 11 ORD ← B V[1:0] ← NEXT	IA ← 11 IB ← 10 ORD ← B V[1:0] ← NEXT	IA ← 10 IB ← 11 ORD ← A V[1:0] ← NEXT	IA ← 10 IB ← 11 ORD ← A V[1:0] ← NEXT
	10	IA ← 11 IB ← NOP ORD ← A V[1:0] ← NEXT	IA ← 11 IB ← 10 ORD ← B V[1:0] ← NEXT	IA ← 11 IB ← 10 ORD ← B V[1:0] ← NEXT	IA ← 10 IB ← NOP STALL ← 1 ORD ← A V[1:0] ← 01
1d0		NOT POSSIBLE	IA ← NOP IB ← 10 STALL ← 1 ORD ← B V[1:0] ← 01	IA ← 10 IB ← NOP STALL ← 1 ORD ← A V[1:0] ← 01	IA ← 10 IB ← NOP STALL ← 1 ORD ← A V[1:0] ← 01

FIG.3

*NOTE:I0 VALID AND I1 NOT VALID WON'T OCCUR BECAUSE THERE IS NO OUT OF ORDER EXECUTION.

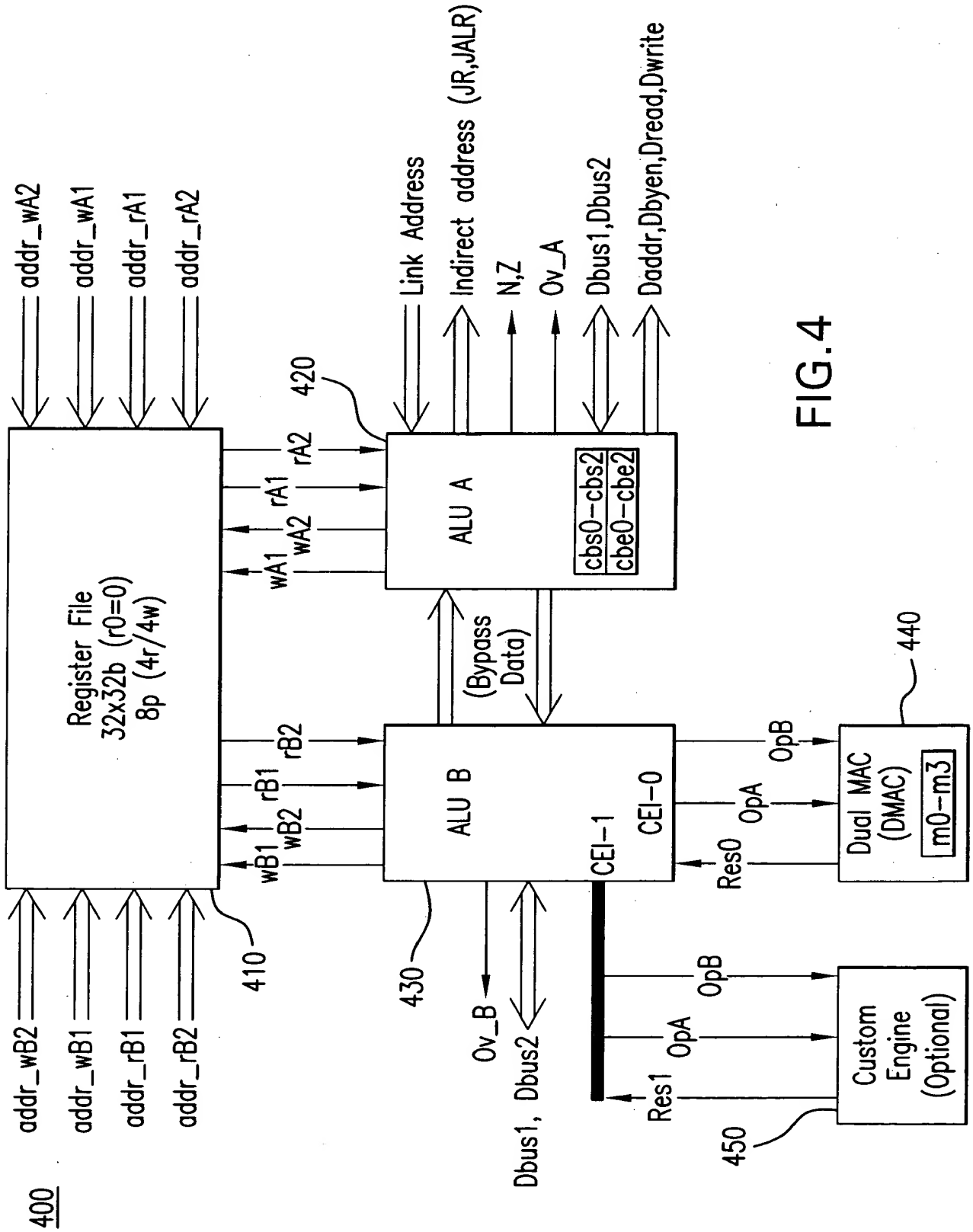

400
addr_wA2
addr_wA1
addr_rA1
addr_rA2
addr_wB2
addr_wB1
addr_rB1
addr_rB2
Register File
32x32b (r0=0)
8p (4r/4w)
410
rA2
rA1
wA2
wA1
rB2
rB1
wB2
wB1
420
ALU A
cbs0–cbs2
cbe0–cbe2
ALU B
CEI–0
CEI–1
430
(Bypass Data)
Link Address
Indirect address (JR,JALR)
N,Z
Ov_A
Dbus1,Dbus2
Daddr,Dbyen,Dread,Dwrite
Ov_B
Dbus1, Dbus2
OpB
OpA
Res0
Dual MAC (DMAC)
m0–m3
440
Res1
Custom Engine (Optional)
450

FIG.4

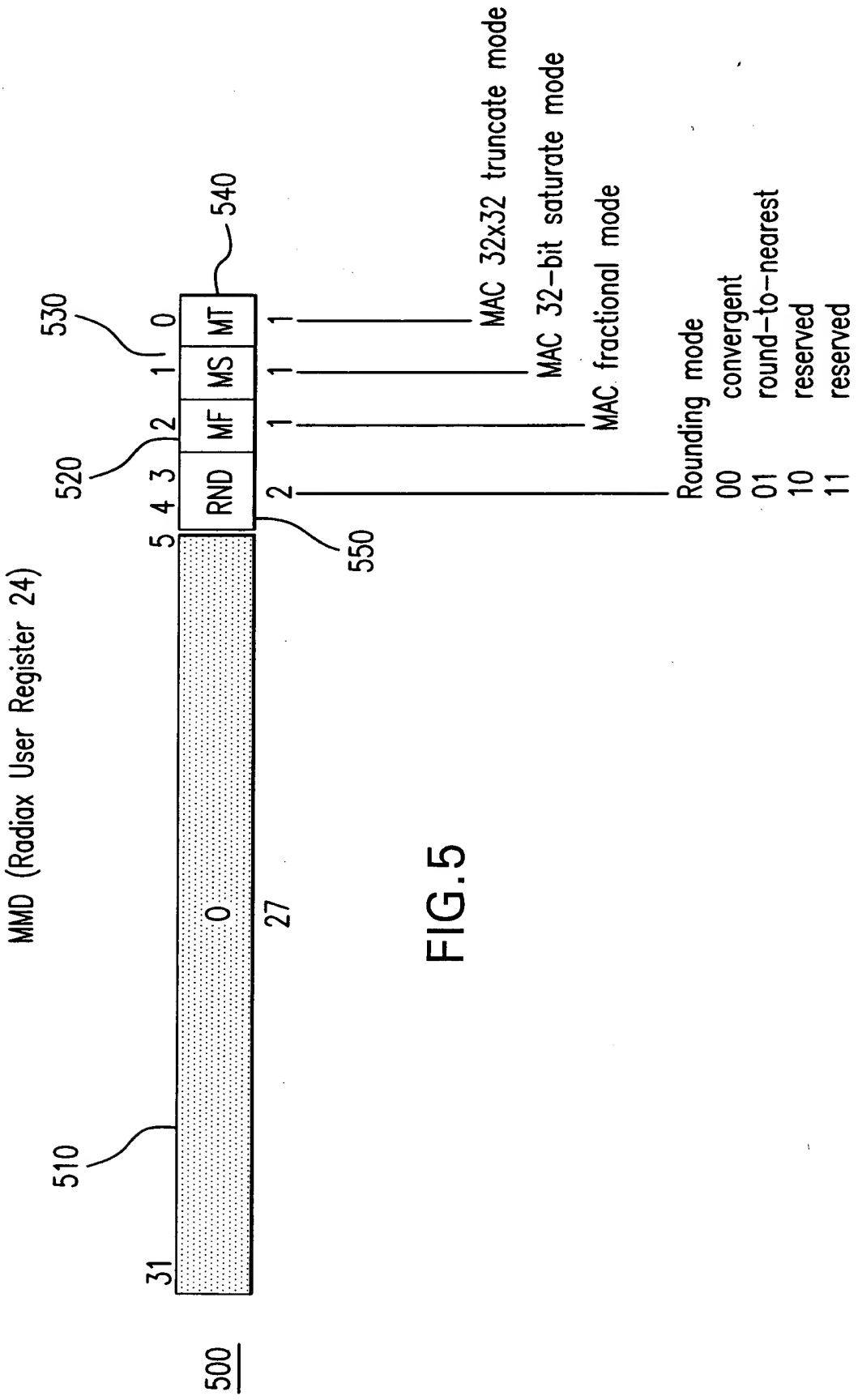

500
MMD (Radiax User Register 24)
510
31
0
27
520
530
540
5 4 3 2 1 0
RND MF MS MT
550
2
1
1
1
MAC fractional mode
MAC 32-bit saturate mode
MAC 32x32 truncate mode
Rounding mode
00 convergent
01 round-to-nearest
10 reserved
11 reserved

FIG.5

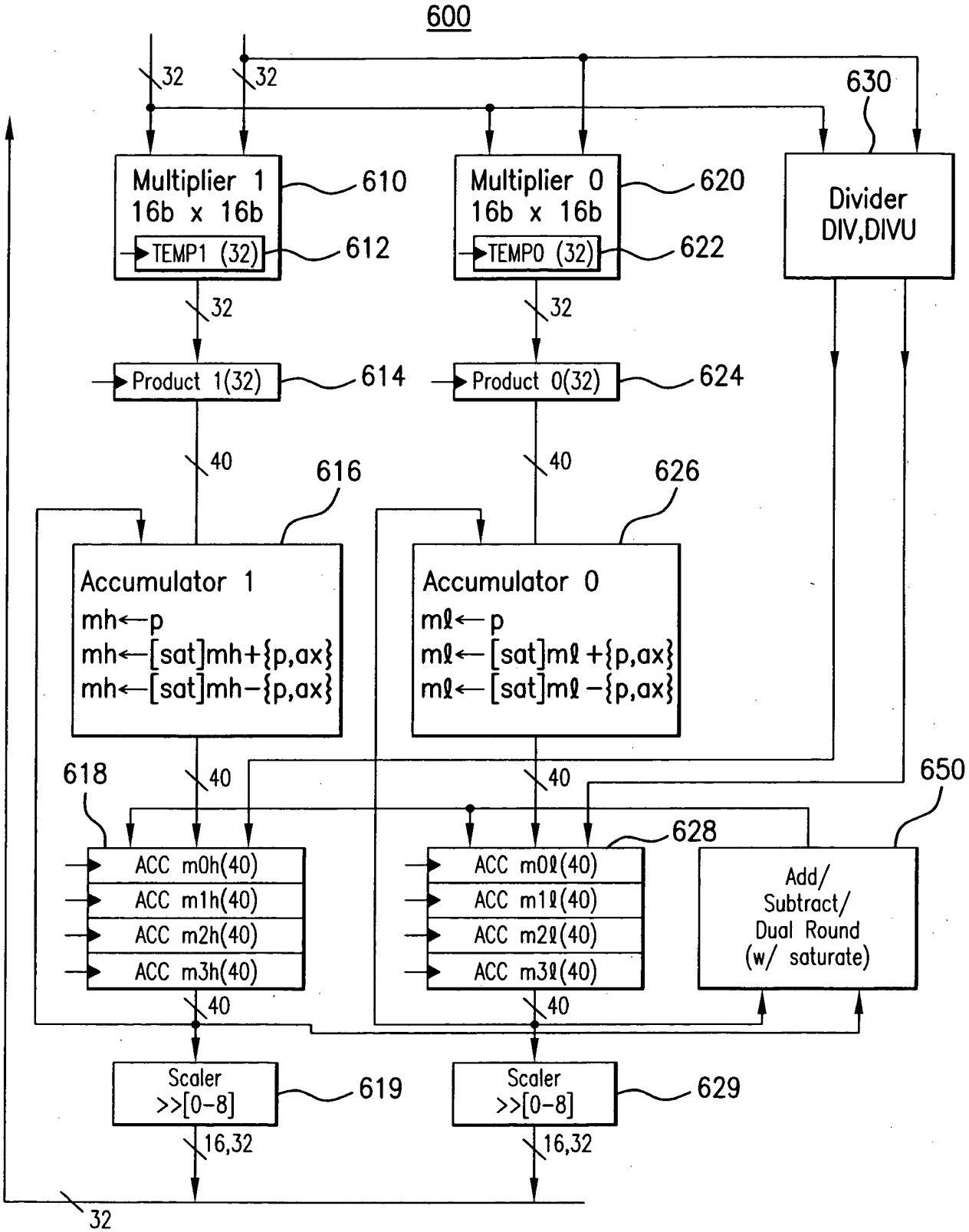

600
32
32
630
Multiplier 1
16b x 16b
610
TEMP1 (32)
612
Multiplier 0
16b x 16b
620
TEMP0 (32)
622
Divider
DIV,DIVU
32
32
Product 1(32)
614
Product 0(32)
624
40
40
616
626
Accumulator 1
mh←p
mh←[sat]mh+{p,ax}
mh←[sat]mh−{p,ax}
Accumulator 0
mℓ←p
mℓ←[sat]mℓ+{p,ax}
mℓ←[sat]mℓ−{p,ax}
618
40
40
650
628
ACC m0h(40)
ACC m1h(40)
ACC m2h(40)
ACC m3h(40)
ACC m0ℓ(40)
ACC m1ℓ(40)
ACC m2ℓ(40)
ACC m3ℓ(40)
Add/
Subtract/
Dual Round
(w/ saturate)
40
40
Scaler
>>[0-8]
619
Scaler
>>[0-8]
629
16,32
16,32
32

FIG.6

- Integer format interpretation:

X=

S	14	13	12			---	0

(radix point)

$$X=-2^{15}xS+\sum_{0}^{14}X[i]2^{i}$$

- Product=P[31:0] is sign-extended to P[39:0]=P[31]^{8} || P[31:0] for accumulation

P=

S	30	29	28			---	0

(radix point)

$$P=-2^{31}xS+\sum_{0}^{30}X[i]2^{i}$$

- Fractional format interpretation:

X=

S	14	13	12			---	0

(radix point)

$$X=-1xS+\sum_{0}^{14}X[i]2^{i-15}$$

Product=P[31:0] is left-shifted one bit and sign-extended to:
P[39:0]=P[30]^{8} || P[30:0] || 0 for accumulation

P=

S	29	28	27			---	zero

(radix point and product left shifted by one)

$$P=-1xS+\sum_{0}^{29}P[i]2^{i-30}$$

FIG.7A

OVERFLOW PROTECTION: GUARD BITS AND SATURATION

- THE LX5280 ACCUMULATOR IMPLEMENTS EIGHT (8) GUARD BITS TO PROTECT AGAINST OVERFLOW. THE ALTERNATIVES OF (i) PRODUCT SCALING OR (ii) INPUT SCALING BY RIGHT SHIFTING, CAUSE LOSS OF PRECISION.

- OPTIONAL SATURATION (MADDA2.S, MSUBA2.S, SUBMA.S) CAN BE USED TO AVOID WRAP-AROUND ON UNDERFLOW OR OVERFLOW OF THE 40-BIT FORMAT (OR 32-BITS IF THAT MODE IS SELECTED IN THE MMD REGISTER):

  IF (RESULT>0 1 1 1 1...1) RESULT=0 1 1 1 1...1

  IF (RESULT<1 0 0 0 0...0) RESULT=1 0 0 0 0...0

- IN 32-BIT SATURATE MODE, THE MAC IMPLEMENTS A FULL 40-BIT SATURATION DETECTOR. THIS ALLOWS FOR THE CASE WHERE THE ACCUMULATOR HOLDS A VALUE GREATER THAN THE MAXIMUM 32-BIT SATURATED VALUE PRIOR TO THE ADDITION (OR SUBTRACTION) WITH SATURATION.

FIG.7B

MAC OUTPUT CONTROL: ROUNDING AND SCALING

- FOR OUTPUT STORAGE, THE 40-BIT ACCUMULATORS MUST BE CONVERTED TO 16-BIT OR 32-BIT FORMAT.
- SCALING

  SINGLE ACCUMULATOR:

  $$RES[31:0] \longleftarrow \{mTh,\ mTl\}\ [31+n:n] \qquad [n=0-8]$$

  DUAL ACCUMULATORS (SELECT HIGH HALF OF EACH, USEFUL FOR FRACTIONAL ARITHMETIC RESULTS):

  $$RES[31:0] \longleftarrow mTh\ [31 + n:16 + n] \parallel mTl\ [31 + n:16 + n][n=0-8]$$

- TO AVOID THE BIAS INTRODUCED BY TRUNCATION, THE ACCUMULATOR CAN BE ROUNDED PRIOR TO OUTPUT SCALING (USEFUL FOR FRACTIONAL ARITHMETIC RESULTS).

  $$\{mT,\ mTh,\ mTl\} \longleftarrow RNDA2\ \{mT,\ mTh,\ mTl\} \qquad [n=0-8]$$

  $\Longrightarrow$ THE ROUNDING MODE IS SELECTABLE IN THE MMD REGISTER

  BIT POSITION 16+n OF EACH ACCUMULATOR IN THE PAIR IS THE LEAST SIGNIFICANT BIT OF PRECISION AFTER ROUNDING

FIG.7C

800

MAC RADIAX INSTRUCTION SUMMARY

INSTRUCTION	SYNTAX AND DESCRIPTION
DUAL MOVE TO ACCUMULATOR	*MTA2 [.G] rS, {mD, mDh, mDℓ}* IF MTA2, AND mDh(mDℓ) IS SELECTED, SIGN-EXTEND THE CONTENTS OF GENERAL REGISTER rS TO 40-BITS AND MOVE TO ACCUMULATOR REGISTER mDh(mDℓ). IF MTA2, AND mD IS SELECTED, UPDATE BOTH mDh AND mDℓ WITH 40-BIT, SIGN-EXTENDED CONTENTS OF THE SAME rS. IF MTA2.G IS SELECTED, THE ACCUMULATOR REGISTER BITS [39:32] ARE UPDATED WITH rS [31:24]; BITS [31:00] OF THE ACCUMULATOR ARE UNCHANGED. (THE .G OPTION IS USED TO RESTORE THE UPPER-BITS OF THE ACCUMULATOR FROM THE GENERAL REGISTER FILE; TYPICALLY, FOLLOWING AN EXCEPTION.)
MOVE FROM ACCUMULATOR	*MFA rD, {mTh, mTℓ} [,n]* MOVE THE CONTENTS OF ACCUMULATOR REGISTER mTh OR ACCUMULATOR REGISTER mTℓ TO REGISTER rD WITH OPTIONAL RIGHT SHIFT. BITS [31+n:n] FROM THE ACCUMULATOR REGISTER ARE TRANSFERRED TO rD[31:00]. THE RANGE n=0-8 IS PERMITTED FOR THE OUTPUT ALIGNMENT SHIFT AMOUNT. IN THE CASE OF n=0, THE FIELD MAY BE OMITTED.
DUAL MOVE FROM ACCUMULATOR	*MFA2 rD, mT [,n]* MOVE THE CONTENTS OF THE UPPER HALVES OF ACCUMULATOR REGISTER PAIR mT TO REGISTER rD WITH OPTIONAL RIGHT SHIFT. THE rD[31:16] ARE TAKEN FROM mTH AND rD[15:00] FROM THE CORRESPONDING mTℓ. mTh[31+n: 16+n] || mTℓ[31+n: 16+n] FROM THE ACCUMULATOR REGISTER PAIR ARE TRANSFERRED TO rD[31:00]. THE RANGE n=0 -8 IS PERMITTED FOR THE OUTPUT ALIGNMENT SHIFT AMOUNT. IN THE CASE OF n=0, THE FIELD MAY BE OMITTED.
DIVIDE	*DIVA mD, rS, rT* THE CONTENTS OF REGISTER rS IS DIVIDED BY rT, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. THE REMAINDER IS SIGN-EXTENDED TO 40-BITS AND STORED IN mDh AND THE QUOTIENT IS SIGN-EXTENDED TO 40-BITS AND STORED IN mDℓ. m0h[31:00] IS ALSO CALLED HI. m0ℓ[31:00] IS ALSO CALLED LO.
DIVIDE UNSIGNED	*DIVAU mD, rS, rT* THE CONTENTS OF REGISTER rS IS DIVIDED BY rT, TREATING THE OPERANDS AS UNSIGNED VALUES. THE REMAINDER IS ZERO-EXTENDED TO 40-BITS AND STORED IN mDh AND THE QUOTIENT IS ZERO-EXTENDED TO 40-BITS AND STORED IN mDℓ. m0h[31:00] IS ALSO CALLED HI. m0ℓ[31:00] IS ALSO CALLED LO.
MULTIPLY (32-BIT)	*MULTA mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. THE UPPER 32-BITS OF THE 64-BIT PRODUCT IS SIGN-EXTENDED TO 40-BITS AND STORED IN mDh AND THE LOWER 32-BITS IS ZERO-EXTENDED TO 40-BITS AND STORED IN THE CORRESPONDING mDl. m0h[31:00] IS ALSO CALLED HI. m0ℓ[31:00] IS ALSO CALLED LO. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE PRODUCT IS LEFT SHIFTED BY ONE BIT, AND FURTHERMORE, IF BOTH OPERANDS ARE -1 THEN THE PRODUCT IS SET TO POSITIVE SIGNED, ALL ONES FRACTION, PRIOR TO THE SHIFT. IF BOTH MMD[MT]AND MMD[MF] ARE 1, THE RESULT IS UNDEFINED.

FIG.8A

800

INSTRUCTION	SYNTAX AND DESCRIPTION
MULTIPLY UNSIGNED (32-BIT)	*MULTAU mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT, TREATING THE OPERANDS AS UNSIGNED VALUES. THE UPPER 32-BITS OF THE 64-BIT PRODUCT IS ZERO-EXTENDED TO 40-BITS AND STORED IN mDh AND THE LOWER 32-BITS IS ZERO-EXTENDED TO 40-BITS AND STORED IN THE CORRESPONDING mDl. mOh[31:00] IS ALSO CALLED HI. mOℓ[31:00] IS ALSO CALLED LO. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE RESULT IS UNDEFINED.
DUAL MULTIPLY (16-BIT)	*MULTA2 {mD, mDh, mDℓ}, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF THE DESTINATION REGISTER IS mDh, rS[31:16] IS MULTIPLIED BY rT[31:16] AND THE PRODUCT IS SIGN-EXTENDED TO 40-BITS AND STORED IN mDh. IF THE DESTINATION REGISTER IS mDℓ, rS[15:00] IS MULTIPLIED BY rT[15:00] AND THE PRODUCT IS SIGN-EXTENDED TO 40-BITS AND STORED IN mDℓ. IF THE DESTINATION IS mD, BOTH OPERATIONS ARE PERFORMED AND THE TWO PRODUCTS ARE STORED IN THE ACCUMULATOR REGISTER PAIR mD. IF MMD[MF] IS 1, THEN EACH PRODUCT IS LEFT SHIFTED BY ONE BIT, AND FURTHERMORE, FOR EACH MULTIPLY, IF BOTH OPERANDS ARE -1 THEN THE PRODUCT IS SET TO POSITIVE SIGNED, ALL ONES FRACTION.
DUAL MULTIPLY AND NEGATE (16-BIT)	*MULNA2 {mD, mDh, mDℓ}, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF THE DESTINATION REGISTER IS mDh, rS[31:16] IS MULTIPLIED BY rT[31:16] AND THE PRODUCT IS SIGN-EXTENDED TO 40-BITS, NEGATED (I.E. SUBTRACTED FROM ZERO) AND STORE IN mDh. IF THE DESTINATION REGISTER IS mDℓ, rS[15:00] IS MULTIPLIED BY rT[15:00] AND THE PRODUCT IS SIGN-EXTENDED TO 40-BITS, NEGATED (I.E. SUBTRACTED FROM ZERO) AND STORED IN mDℓ. IF THE DESTINATION IS mD, BOTH OPERATIONS ARE PERFORMED AND THE TWO PRODUCTS ARE STORED IN THE ACCUMULATOR REGISTER PAIR mD. IF MMD[MF] IS 1, THEN EACH PRODUCT IS LEFT SHIFTED BY ONE BIT PRIOR TO SIGN-EXTENSION AND NEGATION, AND FURTHERMORE, FOR EACH MULTIPLY, IF BOTH OPERANDS ARE -1 THEN THE PRODUCT IS SET TO POSITIVE SIGNED, ALL ONES FRACTION PRIOR TO SIGN-EXTENSION AND NEGATION.
COMPLEX MULTIPLY,	*CMULTA mD, rS, rT* rS[31:16] IS INTERPRETED AS THE REAL PART OF A COMPLEX NUMBER. rS[15:00] IS INTERPRETED AS THE IMAGINARY PART OF THE SAME COMPLEX NUMBER. SIMILARLY FOR THE CONTENTS OF GENERAL REGISTER rT. AS THE RESULT OF CMULTA, mDh IS UPDATED WITH THE REAL PART OF THE PRODUCT, SIGN-EXTENDED TO 40-BITS AND mDℓ IS UPDATED WITH THE IMAGINARY PART OF THE PRODUCT, SIGN-EXTENDED TO 40-BITS. IF MMD[MF] IS 1, THEN EACH PRODUCT IS LEFT SHIFTED BY ONE BIT, AND FURTHERMORE, FOR EACH MULTIPLY, IF BOTH OPERANDS ARE -1 THEN THE PRODUCT IS SET TO POSITIVE SIGNED, ALL ONES FRACTION, PRIOR TO THE ADDITION OF TERMS.

FIG.8B

INSTRUCTION	SYNTAX AND DESCRIPTION
32-BIT MULTIPLY-ADD WITH 72-BIT ACCUMULATE	*MADDA mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE PRODUCT IS LEFT SHIFTED BY ONE BIT, AND FURTHERMORE, IF BOTH OPERANDS ARE-1 THEN THE PRODUCT IS SET TO A POSITIVE SIGNED, ALL ONES FRACTION. IF BOTH MMD[MT] AND MMD[MF] ARE 1, THEN THE RESULT OF THE MULTIPLY IS UNDEFINED. THE 64-BIT PRODUCT IS SIGN-EXTENDED TO 72-BITS AND ADDED TO THE CONCATENATION mDh[39:0] || mDℓ[31:0], IGNORING mDℓ[39:32]. THE LOWER 32 BITS OF THE RESULT ARE ZERO-EXTENDED TO 40-BITS AND STORED INTO mDℓ. THE UPPER 40-BITS OF THE RESULT ARE STORED INTO mDh.
32-BIT UNSIGNED MULTIPLY-ADD WITH 72-BIT ACCUMULATE	*MADDAU mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT TREATING THE OPERANDS AS UNSIGNED VALUES. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE RESULT OF THE MULTIPLY IS UNDEFINED. THE 64-BIT PRODUCT IS ZERO-EXTENDED TO 72-BITS AND ADDED TO THE CONCATENATION mDh[39:0] || mDℓ[31:0], IGNORING mDℓ[39:32]. THE LOWER 32 BITS OF THE RESULT ARE ZERO-EXTENDED TO 40-BITS AND STORED INTO mDℓ. THE UPPER 40-BITS OF THE RESULT ARE STORED INTO mDh.
DUAL MULTIPLY-ADD, OPTIONAL SATURATION	*MADDA2[.S] {mD, mDh, mDℓ}, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT AND ADDED TO AN ACCUMULATOR REGISTER, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF THE DESTINATION REGISTER IS mDh, rS[31:16] IS MULTIPLIED BY rT[31:16] THEN SIGN-EXTENDED AND ADDED TO mDh[39:00]. IF THE DESTINATION REGISTER IS mDℓ, rS[15:00] IS MULTIPLIED BY rT[15:00] THEN SIGN-EXTENDED AND ADDED TO mDℓ[39:00]. IF THE DESTINATION IS mD, BOTH OPERATIONS ARE PERFORMED AND THE TWO RESULTS ARE STORED IN THE ACCUMULATOR REGISTER PAIR mD. IF MADDA2.S THE RESULT OF EACH ADDITION IS SATURATED BEFORE STORAGE IN THE ACCUMULATOR REGISTER. THE MULTIPLIES ARE SUBJECT TO MMD[MF] AS IN MULTA2. THE SATURATION POINT IS SELECTED AS EITHER 40 OR 32 BITS BY MMD[MS].
32-BIT MULTIPLY-SUBTRACT WITH 72-BIT ACCUMULATE	*MSUBA mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE PRODUCT IS LEFT SHIFTED BY ONE BIT, AND FURTHERMORE, IF BOTH OPERANDS ARE -1 THEN THE PRODUCT IS SET TO A POSITIVE SIGNED, ALL ONES FRACTION. IF BOTH MMD[MT] AND MMD[MF] ARE 1, THEN THE RESULT OF THE MULTIPLY IS UNDEFINED. THE 64-BIT PRODUCT IS SIGN-EXTENDED TO 72-BITS AND SUBTRACTED FROM THE CONCATENATION mDh[39:0] || mDℓ[31:0], IGNORING mDℓ[39:32]. THE LOWER 32 BITS OF THE RESULT ARE ZERO-EXTENDED TO 40-BITS AND STORED INTO mDℓ. THE UPPER 40-BITS OF THE RESULT ARE STORED INTO mDh.

FIG.8C

INSTRUCTION	SYNTAX AND DESCRIPTION
32-BIT UNSIGNED MULTIPLY-SUBTRACT WITH 72-BIT ACCUMULATE	*MSUBAU mD, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT TREATING THE OPERANDS AS UNSIGNED VALUES. IF MMD[MT] IS 1, THEN THE PARTIAL PRODUCT rS[15:00] x rT[15:00] IS NOT INCLUDED IN THE TOTAL PRODUCT. IF MMD[MF] IS 1, THEN THE RESULT OF THE MULTIPLY IS UNDEFINED. THE 64-BIT PRODUCT IS ZERO-EXTENDED TO 72-BITS AND SUBTRACTED FROM THE CONCATENATION mDh[39:0] || mDℓ[31:0], IGNORING mDℓ[39:32]. THE LOWER 32 BITS OF THE RESULT ARE ZERO-EXTENDED TO 40-BITS AND STORED INTO mDℓ. THE UPPER 40-BITS OF THE RESULT ARE STORED INTO mDh.
DUAL MULTIPLY-SUB, OPTIONAL SATURATION	*MSUBA2[.S] {mD, mDH, mDℓ}, rS, rT* THE CONTENTS OF REGISTER rS IS MULTIPLIED BY rT AND SUBTRACTED FROM AN ACCUMULATOR REGISTER, TREATING THE OPERANDS AS SIGNED 2's COMPLEMENT VALUES. IF THE DESTINATION REGISTER IS mDh, rS[31:16] IS MULTIPLIED BY rT[31:16] THEN SIGN-EXTENDED AND SUBTRACTED FROM mDh[39:00]. IF THE DESTINATION REGISTER IS mDℓ, rS[15:00] IS MULTIPLIED BY rT[15:00] THEN SIGN-EXTENDED AND SUBTRACTED FROM mDℓ[39:00]. IF THE DESTINATION IS mD, BOTH OPERATIONS ARE PERFORMED AND BOTH RESULTS ARE STORED IN THE ACCUMULATOR REGISTER PAIR mD. IF MSUBA2.S THE RESULT OF EACH SUBTRACTION IS SATURATED BEFORE STORAGE IN THE ACCUMULATOR REGISTER.
ADD ACCUMULATORS	*ADDMA[.S] mD{h,ℓ}, mT{h,ℓ}* THE CONTENTS OF ACCUMULATOR mTh OR mTl IS ADDED TO THE CONTENTS OF ACCUMULATOR mSh OR mSℓ, TREATING BOTH REGISTERS AS SIGNED 40-BIT VALUES. mDh OR mDℓ IS UPDATED WITH THE RESULT. IF ADDMA.S, THE RESULT IS SATURATED BEFORE STORAGE. THE SATURATION POINT IS SELECTED AS EITHER 40 OR 32 BITS BY MMD[MS].
SUBTRACT ACCUMULATORS	*SUBMA[.S] mD{h,ℓ}, mS{h,ℓ}, mT{h,ℓ}* THE CONTENTS OF ACCUMULATOR mTh OR mTℓ IS SUBTRACTED FROM THE CONTENTS OF ACCUMULATOR mSh OR mSℓ, TREATING BOTH REGISTERS AS SIGNED 40-BIT VALUES. mDh OR mDℓ IS UPDATED WITH THE RESULT. IF SUBMA.S, THE RESULT IS SATURATED BEFORE STORAGE. THE SATURATION POINT IS SELECTED AS EITHER 40 OR 32 BITS BY MMD[MS].
DUAL ROUND	*RNDA2 {mT, mTh, mTℓ} [,n]* THE ACCUMULATOR REGISTER mTh OR mTℓ IS ROUNDED, THEN UPDATED. IF mT, THE ACCUMULATOR REGISTER PAIR mTh/mTℓ ARE EACH ROUNDED, THEN UPDATED. THE ROUNDING MODE IS SELECTED IN MMD FIELD "RND". THE LEAST SIGNIFICANT BIT OF PRECISION IN THE ACCUMULATOR REGISTER AFTER ROUNDING IS: 16+n. BITS [15+n:00] ARE ZEROED. THE RANGE n=0-8 IS PERMITTED FOR THE OUTPUT ALIGNMENT SHIFT AMOUNT. IN THE CASE OF n=0, THE FIELD MAY BE OMITTED.

NOMENCLATURE:

rS, rT = r0-r31

mD = mDh \|\| mDℓ; ALSO FOR mT
mDh = m0h-m3h; ALSO FOR mSh, mTh
mDℓ = m0ℓ-m3ℓ; ALSO FOR mSh, mTh
HI = m0h[31:00]
LO = m0ℓ[31:00]

FIG.8D

900

ASSIGNMENT OF INSTRUCTIONS OF PIPE A, PIPE B

	Pipe A	Pipe B
	THE LOAD/STORE PIPE	THE MAC PIPE
MIPS 32-BIT GENERAL INSTRUCTIONS	MIPS 32-BIT GENERAL INSTRUCTIONS EXCEPT: CE1 CUSTOM ENGINE OPCODES, MULT(U), DIV(U), MFHI, MFLO, MTHI, MTLO, MAD(U), MSUB(U)	MULT(U), DIV(U), MFHI, MFLO, MTHI, MTLO, MAD(U), MSUB(U) CE1 CUSTOM ENGINE OPCODES, MIPS 32-BIT ALU INSTRUCTIONS NOTE: NO LOAD OR STORE INSTRUCTIONS
MIPS 32-BIT CONTROL INSTRUCTIONS	J, JAL, JR, JALR, JALX SYSCALL, BREAK, ALL BRANCH INSTRUCTIONS, ALL COPz, SWCz, LWCz	
MIPS16 INSTRUCTIONS (NO DOUBLEWORD INSTRUCTIONS)	ALL MIPS16 INSTRUCTIONS EXCEPT: MULT(U), DIV(U), MFHI, MFLO	MULT(U), DIV(U), MFHI, MFLO
EJTAG INSTRUCTIONS	DERET, SDBBP (INCLUDING MIPS16 SDBBP)	
LEXRA CONTROL INSTRUCTIONS	MTRU, MFRU, MTRK, MFRK, MTLXC0,MFLXC0	
LEXRA VECTOR ADDRESSING	LT, ST, LTP, LWP, LHP(U), LBP(U), STP, SWP, SHP, SBP	
LEXRA MAC INSTRUCTIONS		MTA2, MFA, MFA2, MULTA, MULTA2, MULNA2, CMULTA, MADDA, MSUBA, ADDMA, SUBMA, DIVA, RNDA2
LEXRA EXTENSIONS TO MIPS ALU INSTRUCTIONS	SLLV2, SRLV2, SRAV2 ADDR, ADDR2, SUBR, SUBR2, SLTR2	SLLV2, SRLV2, SRAV2, ADDR, ADDR2, SUBR, SUBR2, SLTR2
NEW LEXRA ALU OPERATIONS	MIN, MIN2, MAX, MAX2, ABSR, ABS2, CLS, MUX2, BITREV, CMVEQZ, CMVNEZ	MIN, MIN2, MAX, MAX2, ABSR, ABS2, CLS, MUX2, BITREV, CMVEQZ, CMVNEZ

FIG.9

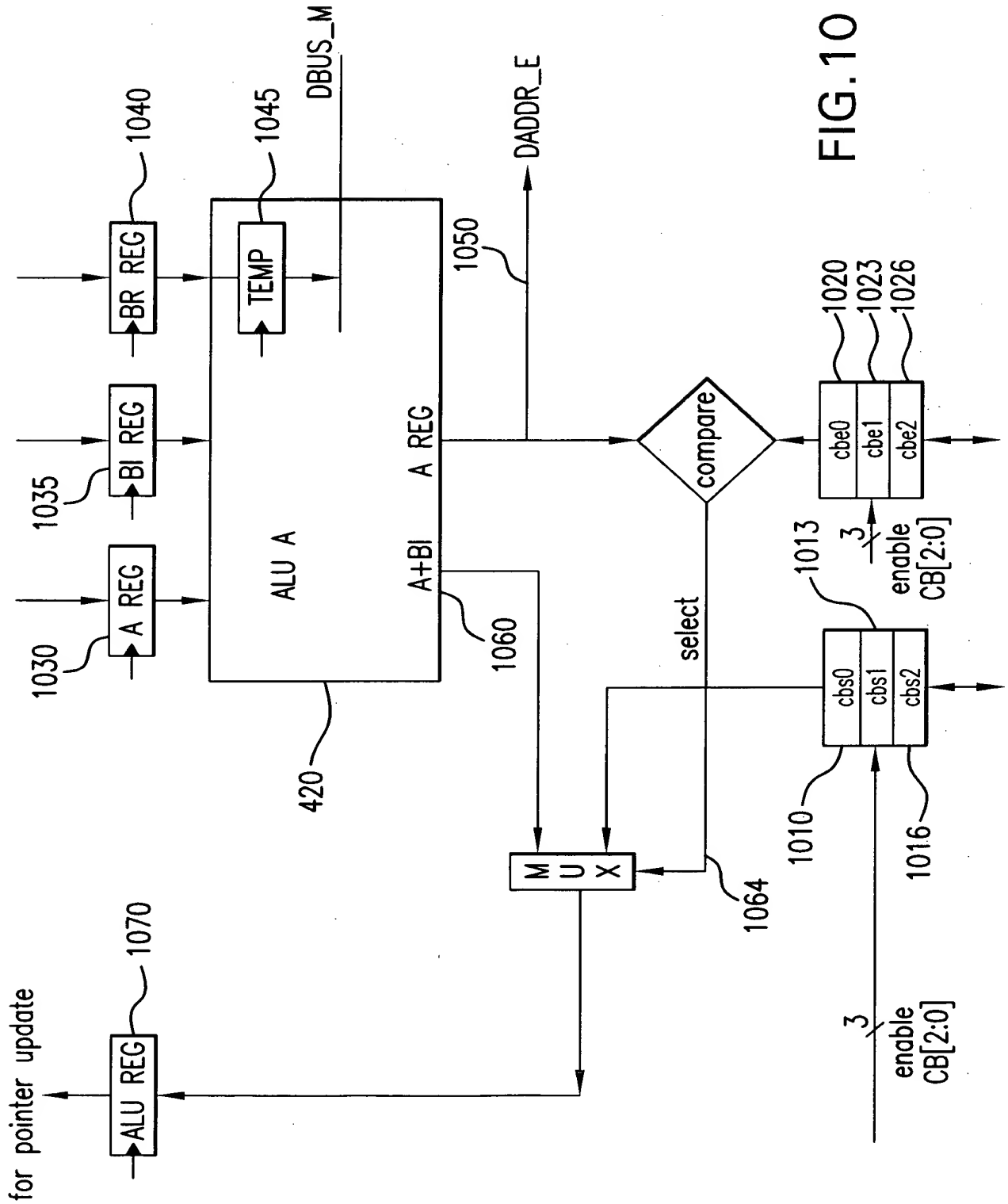

DBUS_M
DADDR_E
1040
1045
1050
1020
1023
1026
BR REG
TEMP
BI REG
A REG
ALU A
A REG
A+BI
compare
cbe0
cbe1
cbe2
1035
1030
1060
1013
3
enable
CB[2:0]
select
cbs0
cbs1
cbs2
420
1010
1016
MUX
1064
3
enable
CB[2:0]
1070
ALU REG
for pointer update

FIG. 10

1100

VECTOR ADDRESSING INSTRUCTION SUMMARY

INSTRUCTION	SYNTAX AND DESCRIPTION
LOAD TWINWORD	*LT rT, DISPLACEMENT(BASE)* THE DISPLACEMENT, IN BYTES, IS A SIGNED 14-BIT QUANTITY THAT MUST BE DIVISIBLE BY 8 (SINCE IT OCCUPIES ONLY 11 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE DISPLACEMENT TO 32-BITS AND ADD TO THE CONTENTS OF REGISTER *BASE* TO FORM THE ADDRESS *TEMP*. LOAD CONTENTS OF WORD ADDRESSED BY *TEMP* INTO REGISTER rT (WHICH MUST BE AN EVEN REGISTER). LOAD CONTENTS OF WORD ADDRESSED BY *TEMP*+4 INTO REGISTER rT+1.
STORE TWINWORD	*ST rT, DISPLACEMENT(BASE)* THE DISPLACEMENT, IN BYTES, IS A SIGNED 14-BIT QUANTITY THAT MUST BE DIVISIBLE BY 8 (SINCE IT OCCUPIES ONLY 11 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE DISPLACEMENT TO 32-BITS AND ADD TO THE CONTENTS OF REGISTER *BASE* TO FORM THE ADDRESS *TEMP*. STORE CONTENTS OF REGISTER rT (WHICH MUST BE AN EVEN REGISTER) INTO WORD ADDRESSED BY *TEMP*. STORE CONTENTS OF REGISTER rT+1 INTO WORD ADDRESSED BY *TEMP*+4.
LOAD TWINWORD, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LTP[.Cn] rT, (POINTER)STRIDE* LET *TEMP*=CONTENTS OF REGISTER *POINTER*. LOAD CONTENTS OF WORD ADDRESSED BY *TEMP* INTO REGISTER rT (WHICH MUST BE AN EVEN REGISTER). LOAD CONTENTS OF WORD ADDRESSED BY *TEMP*+4 INTO REGISTER rT+1. THE STRIDE, IN BYTES, IS A SIGNED 11-BIT QUANTITY THAT MUST BE DIVISIBLE BY 8 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
LOAD WORD, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LWP[.Cn] rT, (POINTER)STRIDE* LOAD CONTENTS OF WORD ADDRESSED BY REGISTER *POINTER* INTO REGISTER rT. THE STRIDE, IN BYTES, IS A SIGNED 10-BIT QUANTITY THAT MUST BE DIVISIBLE BY 4 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
LOAD HALFWORD, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LHP[.Cn] rT, (POINTER)STRIDE* LOAD CONTENTS OF SIGN-EXTENDED HALFWORD ADDRESSED BY REGISTER *POINTER* INTO REGISTER rT. THE STRIDE, IN BYTES, IS A SIGNED 9-BIT QUANTITY THAT MUST BE DIVISIBLE BY 2 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
LOAD HALFWORD UNSIGNED, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LHPU[.Cn] rT, (POINTER)STRIDE* LOAD CONTENTS OF ZERO-EXTENDED HALFWORD ADDRESSED BY REGISTER *POINTER* INTO REGISTER rT. THE STRIDE, IN BYTES, IS A SIGNED 9-BIT QUANTITY THAT MUST BE DIVISIBLE BY 2 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.

FIG. 11A

VECTOR ADDRESSING INSTRUCTION SUMMARY

INSTRUCTION	SYNTAX AND DESCRIPTION
LOAD BYTE, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LBP[.Cn] rT, (POINTER)STRIDE* LOAD CONTENTS OF SIGN-EXTENDED BYTE ADDRESSED BY REGISTER *POINTER* INTO REGISTER rT. THE STRIDE, IN BYTES, IS A SIGNED 8-BIT QUANTITY. SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
LOAD BYTE UNSIGNED, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*LBPU[.Cn] rT, (POINTER)STRIDE* LOAD CONTENTS OF ZERO-EXTENDED BYTE ADDRESSED BY REGISTER *POINTER* INTO REGISTER rT. THE STRIDE, IN BYTES, IS A SIGNED 8-BIT QUANTITY. SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS TO REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
STORE TWINWORD, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*STP[.Cn] rT, (POINTER)STRIDE* LET *TEMP*=CONTENTS OF REGISTER *POINTER*. STORE CONTENTS OF REGISTER rT (WHICH MUST BE AN EVEN REGISTER) INTO WORD ADDRESSED BY *TEMP*. STORE CONTENTS OF REGISTER rT+1 INTO WORD ADDRESSED BY *TEMP*+4. THE STRIDE, IN BYTES, IS A SIGNED 11-BIT QUANTITY THAT MUST BE DIVISIBLE BY 8 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
STORE WORD, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*SWP[.Cn] rT, (POINTER)STRIDE* STORE CONTENTS OF REGISTER rT INTO WORD ADDRESSED BY REGISTER *POINTER*. THE STRIDE, IN BYTES, IS A SIGNED 10-BIT QUANTITY THAT MUST BE DIVISIBLE BY 4 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
STORE HALFWORD, POINTER INCREMENT OPTIONAL CIRCULAR BUFFER	*SHP[.Cn] rT, (POINTER)STRIDE* STORE CONTENTS OF REGISTER rT[15:00] INTO 16-BIT HALFWORD ADDRESSED BY REGISTER *POINTER*. THE STRIDE, IN BYTES, IS A SIGNED 9-BIT QUANTITY THAT MUST BE DIVISIBLE BY 2 (SINCE IT OCCUPIES ONLY 8 BITS OF THE INSTRUCTION WORD). SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
STORE BYTE, POINTER INCREMENT, OPTIONAL CIRCULAR BUFFER	*SBP[.Cn] rT, (POINTER)STRIDE* STORE CONTENTS OF REGISTER rT[07:00] INTO BYTE ADDRESSED BY REGISTER *POINTER*. THE STRIDE, IN BYTES, IS A SIGNED 8-BIT QUANTITY. SIGN-EXTEND THE STRIDE TO 32-BITS AND ADD TO CONTENTS OF REGISTER *POINTER* TO FORM NEXT ADDRESS. UPDATE *POINTER* WITH THE CALCULATED NEXT ADDRESS. ".Cn" SELECTS CIRCULAR BUFFER n=0-2. SEE NOTE 2.
MOVE TO RADIAX, USER	*MTRU rT, RADREG* MOVE THE CONTENTS OF REGISTER rT TO ONE OF THE USER RADIAX REGISTERS: cbs0-cbs2, cbe0-cbe2, mmd, lpc0, lpe0, lps0. THIS INSTRUCTION HAS A SINGLE DELAY SLOT BEFORE THE UPDATED REGISTER TAKES EFFECT.

FIG. 11B

INSTRUCTION	SYNTAX AND DESCRIPTION
MOVE FROM RADIAX, USER	*MFRU rT, RADREG* MOVE THE CONTENTS OF THE DESIGNATED USER RADIAX REGISTER (cbs0–cbs2, cbe0–cbe2, mmd, ℓpc0, ℓps0, ℓpe0) TO REGISTER rT.

NOMENCLATURE:

rT = r0–r31, AND MUST BE EVEN FOR LT, ST, LTP[.Cn], STP[.Cn]
BASE, POINTER = r0–r31
STRIDE = 8/9/10/11–BIT SIGNED VALUE (IN BYTES) FOR BYTE/HALFWORD/WORD/TWINWORD OPS.
DISPLACEMENT = 14–BIT SIGNED VALUE, IN BYTES
RADREG = cbs0–cbs2, cbe0–cbe2, mmd, ℓpc0, ℓps0, ℓpe0

NOTES:

1.FOR LTP[.Cn], LWP[.Cn], LHP(U)[.Cn], LBP(U)[.Cn], rT=*POINTER* IS UNSUPPORTED.
2.WHEN A CIRCULAR BUFFER IS SELECTED, THE UPDATE OF THE POINTER REGISTER IS PERFORMED ACCORDING TO THE FOLLOWING ALGORITHM, WHICH DEPENDS ON THE SIGN OF THE STRIDE AND THE GRANULARITY OF THE ACCESS. A STRIDE EXACTLY EQUAL TO 0 IS NOT SUPPORTED:

FOR LBP(U).Cn ADN SBP.Cn:

```
     IF (STRIDE>0 && POINTER[2:0] == 111 && POINTER[31:3] == CBEn)
        THEN POINTER<= CBSn[31:3] || 000
ELSE IF (STRIDE<0 && POINTER[2:0] == 000 && POINTER[31:3] == CBSn)
        THEN POINTER<= CBEn[31:3] || 111
ELSE          POINTER<= POINTER + STRIDE.
```

FOR LHP(U).Cn AND SHP.Cn

```
     IF (STRIDE>0 && POINTER[2:0] == 11x && POINTER[31:3] == CBEn)
        THEN POINTER<= CBSn[31:3] || 000
ELSE IF (STRIDE<0 && POINTER[2:0] == 00x && POINTER[31:3] == CBSn)
        THEN POINTER<= CBEn[31:3] || 110
ELSE          POINTER<= POINTER + STRIDE.
```

FOR LWP.Cn AND SWP.Cn

```
     IF (STRIDE>0 && POINTER[2:0] == 1xx && POINTER[31:3] == CBEn)
        THEN POINTER<= CBSn[31:3] || 000
ELSE IF (STRIDE<0 && POINTER[2:0] == 0xx && POINTER[31:3] == CBSn)
        THEN POINTER<= CBEn[31:3] || 100
ELSE          POINTER<= POINTER + STRIDE.
```

FOR LTP.Cn AND STP.Cn

```
     IF (STRIDE>0       && POINTER[31:3] == CBEn)
        THEN POINTER<= CBSn[31:3] || 000
ELSE IF (STRIDE<0       && POINTER[31:3] == CBSn)
        THEN POINTER<= CBEn[31:3] || 000
ELSE          POINTER<= POINTER + STRIDE.
```

FIG. 11C

1200

EXTENSIONS TO MIPS ALU OPERATIONS

INSTRUCTION	SYNTAX AND DESCRIPTION
DUAL SHIFT LEFT LOGICAL VARIABLE	*SLLV2* *rD, rT, rS* THE CONTENTS OF rT[31:16] AND THE CONTENTS OF rT[15:00] ARE INDEPENDENTLY SHIFTED LEFT BY THE NUMBER OF BITS SPECIFIED BY THE LOW ORDER FOUR BITS OF THE CONTENTS OF GENERAL REGISTER rS, INSERTING ZEROS INTO THE LOW ORDER BITS OF rT[31:16] AND rT[15:00]. FOR SLLV2, THE HIGH AND LOW RESULTS ARE CONCATENATED AND PLACED IN REGISTER rD. (NOTE THAT A [.S] OPTION IS NOT PROVIDED BECAUSE THIS IS A *LOGICAL* RATHER THAN *ARITHMETIC* SHIFT AND THUS THE CONCEPT OF ARITHMETIC OVERFLOW IS NOT RELEVANT.)
DUAL SHIFT RIGHT LOGICAL VARIABLE	*SRLV2* *rD, rT, rS* THE CONTENTS OF rT[31:16] AND THE CONTENTS OF rT[15:00] ARE INDEPENDENTLY SHIFTED RIGHT BY THE NUMBER OF BITS SPECIFIED BY THE LOW ORDER FOUR BITS OF THE CONTENTS OF GENERAL REGISTER rS, INSERTING ZEROS INTO THE HIGH ORDER BITS OF rT[31:16] AND rT[15:00]. THE HIGH AND LOW RESULTS ARE CONCATENATED AND PLACED IN REGISTER rD. (NOTE THAT A [.S] OPTION IS NOT PROVIDED BECAUSE THIS IS A *LOGICAL* RATHER THAN *ARITHMETIC* SHIFT AND THUS THE CONCEPT OF ARITHMETIC OVERFLOW IS NOT RELEVANT.)
DUAL SHIFT RIGHT ARITHMETIC VARIABLE	*SRAV2* *rD, rT, rS* THE CONTENTS OF rT[31:16] AND THE CONTENTS OF rT[15:00] ARE INDEPENDENTLY SHIFTED RIGHT BY THE NUMBER OF BITS SPECIFIED BY THE LOW ORDER FOUR BITS OF THE CONTENTS OF GENERAL REGISTER rS, SIGN-EXTENDING THE HIGH ORDER BITS OF rT[31:16] AND rT[15:00]. THE HIGHT AND LOW RESULTS ARE CONCATENATED AND PLACED IN REGISTER rD. (NOTE THAT A [.S] OPTION IS NOT PROVIDED BECAUSE ARITHMETIC OVERFLOW/UNDERFLOW IS NOT POSSIBLE.
ADD, OPTIONAL SATURATION	*ADDR[.S]* *rD, rS, rT* 32-BIT ADDITION. CONSIDERING BOTH QUANTITIES AS SIGNED 32-BIT INTEGERS, ADD THE CONTENTS OF REGISTER rS TO rT. FOR ADDR, THE RESULT IS PLACED IN REGISTER rD, IGNORING ANY OVERFLOW OR UNDERFLOW. FOR ADDR.S, THE RESULT IS SATURATED TO 0 $\|$ 1^{31} (IF OVERFLOW) OR 1 $\|$ 0^{31} (IF UNDERFLOW) THEN PLACED IN rD.ADDR[.S] WILL NOT CAUSE AN OVERFLOW TRAP.
DUAL ADD, OPTIONAL SATURATION	*ADDR2[.S]* *rD, rS, rT* DUAL 16-BIT ADDITION. CONSIDERING ALL QUANTITIES AS SIGNED 16-BIT INTEGERS, ADD THE CONTENTS OF REGISTER rS[15:00] TO rT[15:00] AND, INDEPENDENTLY ADD THE CONTENTS OF REGISTER rS[31:16] TO rT[31:16]. FOR ADDR2, THE HIGH AND LOW RESULTS ARE CONCATENATED AND PLACED IN REGISTER rD IGNORING ANY OVERFLOW OR UNDERFLOW. FOR ADDR2.S, THE TWO RESULTS ARE INDEPENDENTLY SATURATED TO 0 $\|$ 1^{15} (IF OVERFLOW) OR 1 $\|$ 0^{15} (IF UNDERFLOW) THEN PLACED IN rD.ADDR2[.S] WILL NOT CAUSE AN OVERFLOW TRAP.

FIG. 12A

1200

INSTRUCTION	SYNTAX AND DESCRIPTION
SUBTRACT, OPTIONAL SATURATION	*SUBR[.S] rD, rS, rT* 32-BIT SUBTRACTION. CONSIDERING BOTH QUANTITIES AS SIGNED 32-BIT INTEGERS, SUBTRACT THE CONTENTS OF REGISTER rT FROM THE CONTENTS OF REGISTER rS. FOR SUBR, THE RESULT IS PLACED IN REGISTER rD IGNORING ANY OVERFLOW OR UNDERFLOW. FOR SUBR.S, THE RESULT IS SATURATED TO $0 \| 1^{31}$ (IF OVERFLOW) OR $1 \| 0^{31}$ (IF UNDERFLOW) THEN PLACED IN rD SUBR[.S] WILL NOT CAUSE AN OVERFLOW TRAP.
DUAL SUBRACT, OPTIONAL SATURATION	*SUBR2[.S] rD, rS, rT* DUAL 16-BIT SUBTRACTION. CONSIDERING ALL QUANTITIES AS SIGNED 16-BIT INTEGERS, SUBTRACT THE CONTENTS OF REGISTER rT[15:00] FROM rS[15:00] AND , INDEPENDENTLY SUBTRACT THE CONTENTS OF REGISTER rT[31:16] FROM rS[31:16]. FOR SUBR2, THE HIGH AND LOW RESULTS ARE CONCATENATED AND PLACED IN REGISTER rD IGNORING ANY OVERFLOW OR UNDERFLOW. FOR SUBR2.S, THE TWO RESULTS ARE INDEPENDENTLY SATURATED TO $0 \| 1^{15}$ (IF OVERFLOW) OR $1 \| 0^{15}$ (IF UNDERFLOW) THEN PLACED IN rD. SUBR2[.S] WILL NOT CAUSE AN OVERFLOW TRAP.
DUAL SET ON LESS THAN	*SLTR2 rD, rS, rT* DUAL 16-BIT COMPARISON. CONSIDERING BOTH QUANTITIES AS SIGNED 16-BIT INTEGERS, IF rS[15:00] IS LESS THAN rT[15:00] TO $0^{15} \| 1$, ELSE TO ZERO. INDEPENDENTLY, CONSIDERING BOTH QUANTITIES AS SIGNED 16-BIT INTEGERS, IF rS[31:16] IS LESS THAN rT[31:16] THEN SET rD[31:16] TO $0^{15} \| 1$, ELSE TO ZERO.

NOMENCLATURE:

rD = r0-r31
rS = r0-r31
rT = r0-r31

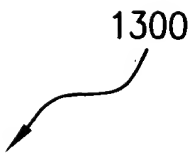
FIG.12B

1300

ALU OPERATIONS

INSTRUCTION	SYNTAX AND DESCRIPTION
MINIMUM	*MIN rD, rS, rT* THE CONTENTS OF THE GENERAL REGISTER rT ARE COMPARED WITH rS CONSIDERING BOTH QUANTITIES AS SIGNED 32-BIT INTEGERS. IF rS<rT OR rS=rT,rS IS PLACED INTO rD. IF, rS>rT,rT IS PLACED INTO rD.
DUAL MINIMUM	*MIN2 rD, rS, rT* THE CONTENTS OF rT[31:16] ARE COMPARED WITH rS[31:16] CONSIDERING BOTH QUANTITIES AS SIGNED 16-BIT INTEGERS. IF rS[31:16]<rT[31:16] OR rS[31:16]= rT[31:16], rS[31:16] IS PLACED INTO rD[31:16]. IF, rS[31:16]>rT[31:16], rT[31:16] IS PLACED INTO rD[31:16]. A SIMILAR, INDEPENDENT OPERATION IS PERFORMED ON rT[15:00] AND rS[15:00] TO DETERMINE rD[15:00].
MAXIMUM	*MAX rD, rS, rT* THE CONTENTS OF THE GENERAL REGISTER rT ARE COMPARED WITH rS CONSIDERING BOTH QUANTITIES AS SIGNED 32-BIT INTEGERS. IF rS>rT OR rS=rT, rS IS PLACED INTO rD. IF, rS<rT, rT IS PLACED INTO rD.
DUAL MAXIMUM	*MAX2 rD, rS, rT* THE CONTENTS OF rT[31:16] ARE COMPARED WITH rS[31:16] CONSIDERING BOTH QUANTITIES AS SIGNED 16-BIT INTEGERS. IF rS[31:16]>rT[31:16] OR rS[31:16]= rT[31:16], rS[31:16] IS PLACED INTO rD[31:16]. IF, rS[31:16]<rT[31:16], rT[31:16] IS PLACED INTO rD[31:16]. A SIMILAR, INDEPENDENT OPERATION IS PERFORMED ON rT[15:00] AND rS[15:00] TO DETERMINE rD[15:00].
ABSOLUTE, OPTIONAL SATURATION	*ABSR[.S] rD, rT* CONSIDERING rT AS A SIGNED 32-BIT INTEGER, IF rT>0, rT IS PLACED INTO rD. IF rT< 0, rT IS PLACED INTO rD. IF ABSR.S AND rT=1 $\|\|$ 0^{31} (THE SMALLEST NEGATIVE NUMBER) THEN 0 $\|\|$ 1^{31} (THE LARGEST POSITIVE NUMBER) IS PLACED INTO rD; OTHERWISE, IF ABSR AND rT=1 $\|\|$ 0^{31}, rT IS PLACED INTO rD.
DUAL ABSOLUTE, OPTIONAL SATURATION	*ABSR2[.S] rD, rT* ABS[.S] OPERATIONS ARE PERFORMED INDEPENDENTLY ON rT[31:16] AND rT[15:00], CONSIDERING EACH TO BE 16-BIT SIGNED INTEGERS. rD IS UPDATED WITH THE ABSOLUTE VALUE OF rT[31:16] CONCATENATED WITH THE ABSOLUTE VALUE OF rT[15:00].
DUAL MUX	*MUX2{[.HH],[.HL],[LH],[.LL]} rD, rS, rT* rD[31:16] IS UPDATED WITH rS[31:16] FOR MUX2.HH OR MUX2.HL rD[31:16] IS UPDATED WITH rS[15:00] FOR MUX2.LH OR MUX2.LL rD[15:00] IS UPDATED WITH rT[31:16] FOR MUX2.HH OR MUX2.LH rD[15:00] IS UPDATED WITH rT[15:00] FOR MUX2.HL OR MUX2.LL
COUNT LEADING SIGN BITS	*CLS rD, rT* THE BINARY-ENCODED NUMBER OF REDUNDANT SIGN BITS OF GENERAL REGISTER rT IS PLACED INTO rD. IF rT[31:30]=10 OR 01, rD IS UPDATED WITH 0. IF rT=0, OR IF rT $=1^{32}$, rD IS UPDATED WITH $0^{27}\|\| 1^{5}$ (DECIMAL 31).

FIG. 13A



ALU OPERATIONS

INSTRUCTION	SYNTAX AND DESCRIPTION
BIT REVERSE	*BITREV* *rD, rT, rS* A BIT-REVERSAL OF THE CONTENTS OF GENERAL REGISTER rT IS PERFORMED. THE RESULT IS THEN SHIFTED RIGHT LOGICALLY BY THE AMOUNT SPECIFIED IN THE LOWER 5-BITS OF THE CONTENTS OF GENERAL REGISTER rS, THEN STORED IN rD.

NOMENCLATURE:

rD = r0-r31
rS = r0-r31
rT = r0-r31

FIG.13B

1400

CONDITIONAL OPERATIONS

INSTRUCTION	SYNTAX AND DESCRIPTION
CONDITIONAL MOVE ON EQUAL ZERO	*CMVEQZ[.H] [.L] rD, rS, rT FULL 32-BIT* IF THE GENERAL REGISTER rT IS EQUAL TO 0, THE GENERAL REGISTER rD IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED. FOR[.H] IF rT[31:16] IS EQUAL TO 0, THE *FULL 32-BIT* GENERAL REGISTER rD[31:00] IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED. FOR [.L] IF rT[15:00] IS EQUAL TO 0, THE *FULL 32-BIT* GENERAL REGISTER rD[31:00] IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED.
CONDITIONAL MOVE ON NOT EQUAL ZERO	*CMVNEZ[.H] [.L] rD, rS, rT* IF THE GENERAL REGISTER rT IS NOT EQUAL TO 0, THE GENERAL REGISTER rD IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED. FOR [.H] IF rT[31:16] IS NOT EQUAL TO 0, THE *FULL 32-BIT* GENERAL REGISTER rD[31:00] IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED. FOR [.L] IF rT[15:00] IS NOT EQUAL TO 0, THE *FULL 32-BIT* GENERAL REGISTER rD[31:00] IS UPDATED WITH rS; OTHERWISE rD IS UNCHANGED.

NOMENCLATURE:

rD = r0–r31
rS = r0–r31
rT = r0–r31

USAGE NOTE:
WHEN COMBINED WITH THE SLT OR SLTR2 INSTRUCTIONS, THE CONDITIONAL MOVE INSTRUCTIONS CAN BE USED TO CONSTRUCT A COMPLETE SET OF CONDITIONAL MOVE MACRO–OPERATIONS. FOR EXAMPLE:

```
if(r3<r4) r1<--r2

  CMVLT r1,r2,r3,r4 ===> SLT    AT,r3,r4
                         CMVNEZ r1,r2,AT
if(r3>=r4)r1<--r2

  CMVGE r1,r2,r3,r4 ===> SLT    AT,r3,r4
                         CMVEQZ r1,r2,AT
if(r3<=r4)r1<-r2

  CMVLE r1,r2,r3,r4 ===> SLT    AT,r4,r3
                         CMVEQZ r1,r2,AT
f(r3>r4) r1<--r2

  CMVGT r1,r2,r3,r4 ===> SLT    AT,r4,r3
                         CMVNEZ r1,r2,AT
```

FIG. 14

CYCLES REQUIRED BETWEEN DUAL MAC INSTRUCTIONS

1st OP / 2nd OP	MULTA(U)		MADDA(U), MSUBA(U)		CMULTA	DIVA(U)	MADDA2[.S], MSUBA2[.S], ADDMA[.S], SUBMA[.S], MULTA2, MULNA2, RNDA2, MTA2	MFA
MULTA(U), MADDA(U),MSUBA(U)	1U		1U		1U	(19T)	-	-
DIVA(U)	(3T)		(4T)		(1T)	19U	-	-
CMULTA, MADDA2[.S], MSUBA2[.S], MULTA2,MULNA2, MTA2	3U		4U		1U	(19T)	-	-
ADDMA[.S], SUBMA[.S], RNDA2	LO 2S 2T	HI 3S 3T	4U		IS IT	(19S) (19T)	-	-
MFA	LO 4S	HI 5S	LO 5S	HI 6S	3S	19S	2S	-

1500

NOTES: -MEANS THE TWO OPS CAN BE ISSUED BACK-TO-BACK.
xU INDICATES UNCONDITIONAL DELAY OF THE INDICATED NUMBER OF CYCLES.
xS INDICATES DELAY ONLY IF (ANY) 2nd OP SOURCE IS THE SAME AS (ANY) 1st OP TARGET (PRODUCER-CONSUMER DEPENDENCY).
xT INDICATES DELAY ONLY IF (ANY) 2nd OP TARGET IS THE SAME AS (ANY) 1st OP TARGET (PRESERVE WRITE AFTER WRITE ORDER).
ITEMS IN PARENTHESIS ARE UNLIKELY TO OCCUR IN ANY USEFUL PROGRAM, WHICH WOULD PROBABLY HAVE AN INTERVENING MFA.
LO/HI INDICATE THAT FOR THE 72-BIT RESULT OF A 32x32 MULT OR MADDA, THE LO 32-BITS (m0ℓ, m1ℓ, ETC.) ARE AVAILABLE ONE CYCLE EARLIER.
DELAY OF "x" CYCLES MEANS THAT IF THE 1st OP ISSUES IN CYCLE N, THEN THE 2nd OP MAY ISSUE IN CYCLE N+x+1.

FIG.15

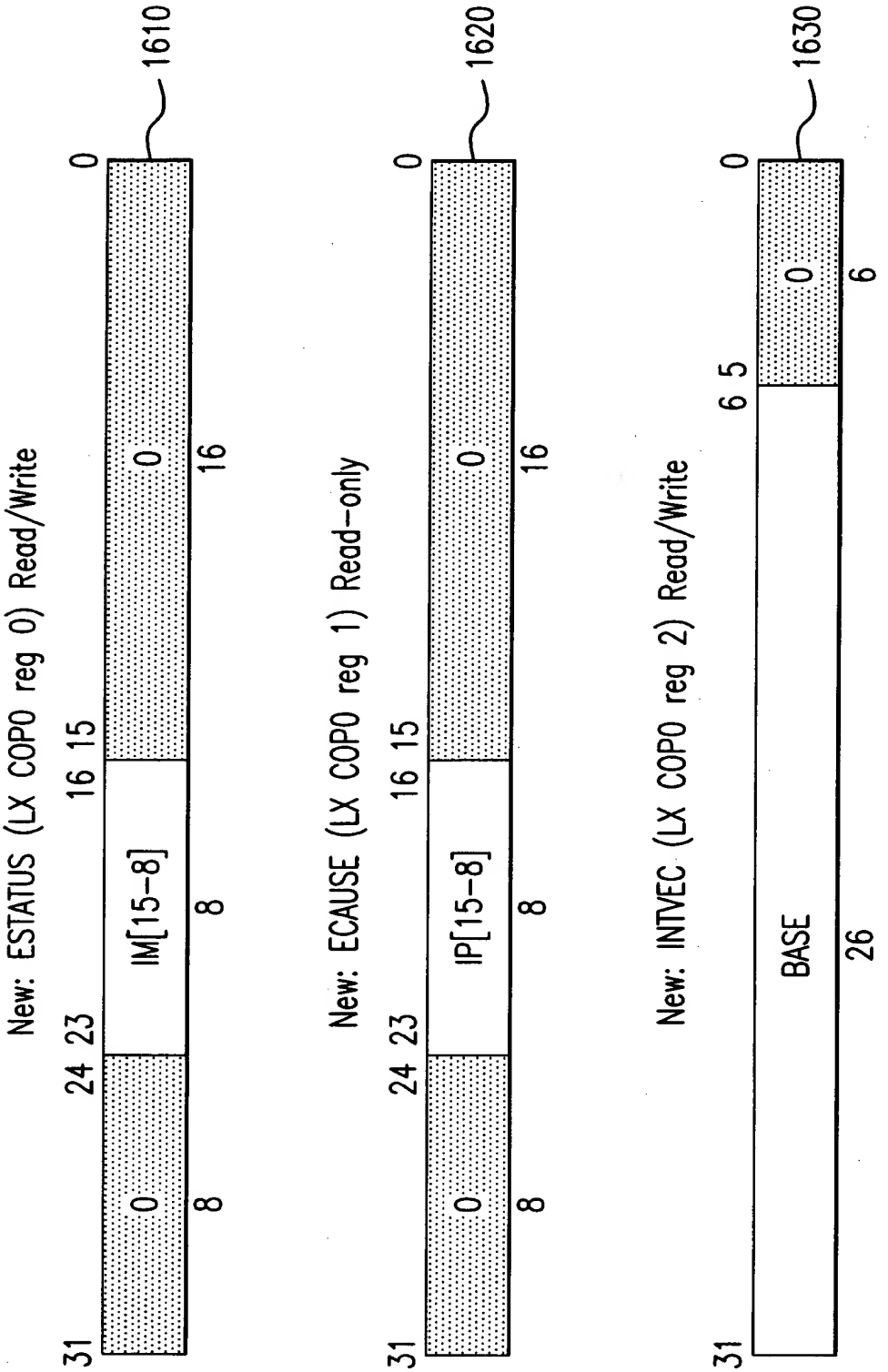
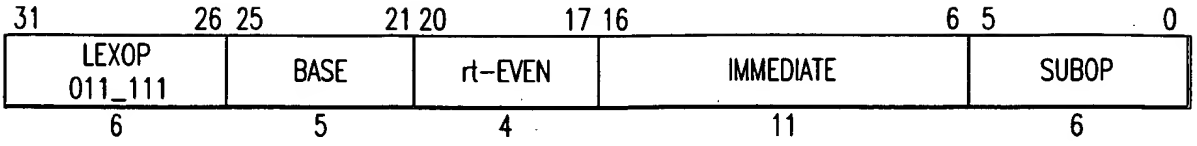
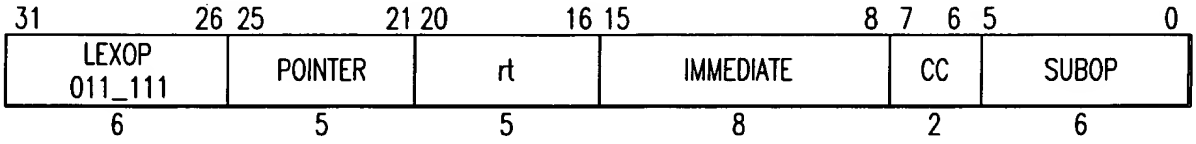

New: ESTATUS (LX COP0 reg 0) Read/Write
31
24 23
16 15
8
0
0
IM[15-8]
0
8
16
0
1610
New: ECAUSE (LX COP0 reg 1) Read-only
31
24 23
16 15
8
0
0
IP[15-8]
0
8
16
0
1620
New: INTVEC (LX COP0 reg 2) Read/Write
31
26
BASE
6 5
0
0
6
0
1630
IM[15-8] is reset to 0.

FIG. 16

I. LOAD/STORE FORMATS



ASSEMBLER MNEMONIC	BASE	rt-EVEN	IMMEDIATE	LEXRA SUBOP
LT	BASE	rt-EVEN	DISPLACEMENT/8	LT
ST	BASE	rt-EVEN	DISPLACEMENT/8	ST



ASSEMBLER MNEMONIC	POINTER	rt	IMMEDIATE	cc	LEXRA SUBOP
LBP[.Cn]	POINTER	rt	STRIDE	cc	LBP
LBPU[.Cn]	POINTER	rt	STRIDE	cc	LBPU
LHP[.Cn]	POINTER	rt	STRIDE/2	cc	LHP
LHPU[.Cn]	POINTER	rt	STRIDE/2	cc	LHPU
LWP[.Cn]	POINTER	rt	STRIDE/4	cc	LWP
LTP[.Cn]	POINTER	rt	STRIDE/8	cc	LTP
SBP[.Cn]	POINTER	rt	STRIDE	cc	SBP
SHP[.Cn]	POINTER	rt	STRIDE/2	cc	SHP
SWP[.Cn]	POINTER	rt	STRIDE/4	cc	SWP
STP[.Cn]	POINTER	rt	STRIDE/8	cc	STP

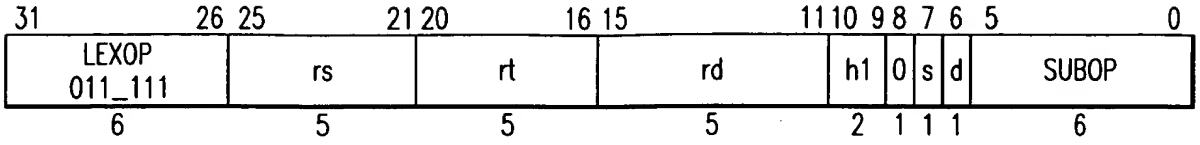
BASE,POINTER,rt — SELECTS GENERAL REGISTER r0-r31.
rt-EVEN — SELECTS GENERAL REGISTER EVEN-ODD PAIR r0/r1,r2/r3,...r30/r31
STRIDE — SIGNED 2s-COMPLEMENT NUMBER IN BYTES. MUST BE AN INTEGRAL NUMBER OF HALFWORDS/WORDS/TWINWORDS FOR THE CORRESPONDING INSTRUCTIONS.

DISPLACEMENT — SIGNED 2s-COMPLEMENT NUMBER IN BYTES. MUST BE AN INTEGRAL NUMBER OF TWINWORDS.

cc
00 — SELECT CIRCULAR BUFFER 0(cbs0,cbe0)
01 — SELECT CIRCULAR BUFFER 1(cbs1,cbe1)
10 — SELECT CIRCULAR BUFFER 2(cbs2,cbe2)
11 — NO CIRCULAR BUFFER SELECTED

FIG. 17A

II. ARITHMETIC FORMAT



ASSEMBLER MNEMONIC	rs	rt	rd	hl	s	d	LEXRA SUBOP
ADDR[.S],ADDR2[.S]	rs	rt	rd	0	s	d	ADDR
SUBR.S,SUBR2[.S]	rs	rt	rd	0	s	d	SUBR
SLTR2	rs	rt	rd	0	0	1	SLTR
SLLV2	rs	rt	rd	0	0	1	SLLV
SRLV2	rs	rt	rd	0	0	1	SRLV
SRAV2	rs	rt	rd	0	0	1	SRAV
MIN,MIN2	rs	rt	rd	0	0	d	MIN
MAX,MAX2	rs	rt	rd	0	0	d	MAX
ABSR[.S],ABSR2[.S]	0	rt	rd	0	s	d	ABSR
MUX2.[LL,LH,HL,HH]	rs	rt	rd	hl	0	1	MUX
CLS	0	rt	rd	0	0	0	CLS
BITREV	rs	rt	rd	0	0	0	BITREV

rs,rt,rd

SELECTS GENERAL REGISTER r0–r31.

s

SELECTS SATURATION OF RESULT. s=1 INDICATES THAT SATURATION IS PERFORMED.

d

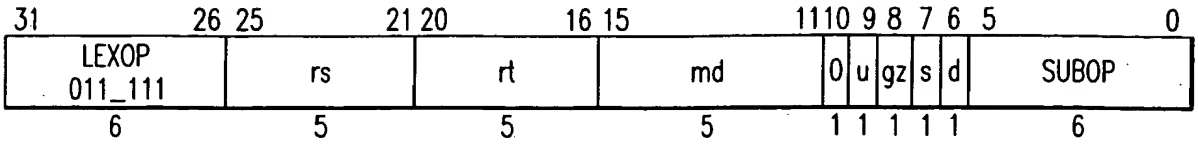
d=1 INDICATES THAT DUAL OPERATIONS ON 16–BIT DATA ARE PERFORMED.

h1 (FOR MUX2)

00 LL:rD=rs[15:00] || rt[15:00]
01 LH:rD=rs[15:00] || rt[31:16]
10 HL:rD=rs[31:16] || rt[15:00]
11 HH:rD=rs[31:16] || rt[31:16]

FIG.17B

III. MAC FORMAT A



ASSEMBLER MNEMONIC	rs	rt	md	u	gz	s	d	LEXRA SUBOP
CMULTA	rs	rt	md	0	0	0	0	CMULTA
DIVA(U)	rs	rt	md	u	0	0	0	DIVA
MULTA(U)	rs	rt	md	u	1	0	0	MADDA
MULTA2	rs	rt	md	0	1	0	1	MADDA
MADDA(U)	rs	rt	md	u	0	0	0	MADDA
MADDA2[.S]	rs	rt	md	0	0	s	1	MADDA
MSUBA(U)	rs	rt	md	u	0	0	0	MSUBA
MSUBA2[.S]	rs	rt	md	0	0	s	1	MSUBA
MULNA2	rs	rt	md	0	1	0	1	MSUBA
MTA2[.G]	rs	0	md	0	g	0	1	MTA

rs,rt SELECTS GENERAL REGISTER r0–r31.

md SELECTS ACCUMULATOR, ONNHL WHERE,

NN=m0–m3
HL
00=RESERVED 01=mN1
10=mNh 11=mN

s SELECTS SATURATION OF RESULT. s=1 INDICATES THAT SATURATION IS PERFORMED.

d d=1 INDICATES THAT DUAL OPERATIONS ON 16–BIT DATA ARE PERFORMED.

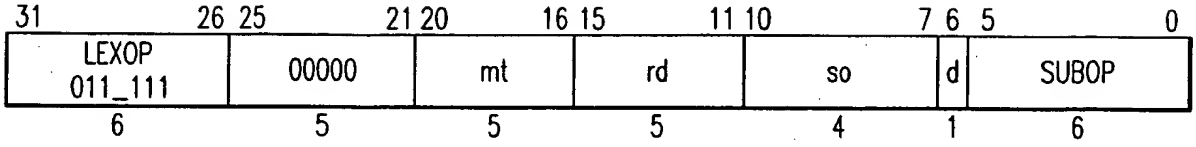
gz FOR MTA2, USED AS "GUARD" BIT. IF g=1,BITS [39:32] OF THE ACCUMULATOR (PAIR) ARE LOADED AND BITS [31:00] ARE UNCHANGED. IF g=0, ALL 40 BITS [39:0] OF THE ACCUMULATOR (OR PAIR) ARE UPDATED.

FOR MADDA,MSUBA,USED A "ZERO" BIT. IF z=1, THE RESULT IS ADDED TO (SUBTRACTED FROM) ZERO RATHER THAN THE PREVIOUS ACCUMULATOR VALUE; THIS PERFORMS A MULTA, MULTA2 OR MULNA2. IF z=0, PERFORMS A MADDA,MSUBA,MADDA2 OR MSUBA2.

u TREAT OPERANDS AS UNSIGNED VALUES (0=SIGNED,1=UNSIGNED)

FIG.17C

IV. MAC FORMAT B



ASSEMBLER MNEMONIC	mt	rd	so	d	LEXRA SUBOP
MFA,MFA2	mt	rd	so	d	MFA
RNDA2	mt	0	so	1	RNDA

rd

SELECTS GENERAL REGISTER r0-r31.

mt SELECTS ACCUMULATOR, ONNHL WHERE,

NN=m0-m3
HL
00=RESERVED
01=mN1
10=mNh
11=mN

d

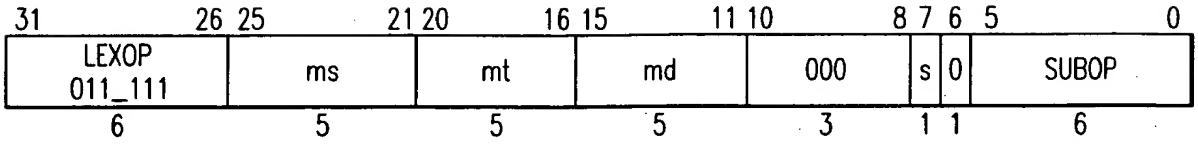
d=1 INDICATES THAT DUAL OPERATIONS ON 16-BIT DATA ARE PERFORMED.

so

ENCODED ("OUTPUT") SHIFT AMOUNT n=0-8 FOR RNDA2,MFA,MFA2 INSTRUCTIONS.

FIG.17D

V. MAC FORMAT C



ASSEMBLER MNEMONIC	ms	mt	md	s	LEXRA SUBOP
ADDMA[.S]	ms	mt	md	s	ADDMA
SUBMA[.S]	ms	mt	md	s	SUBMA

mt,ms,md

SELECTS ACCUMULATOR, ONNHL WHERE,

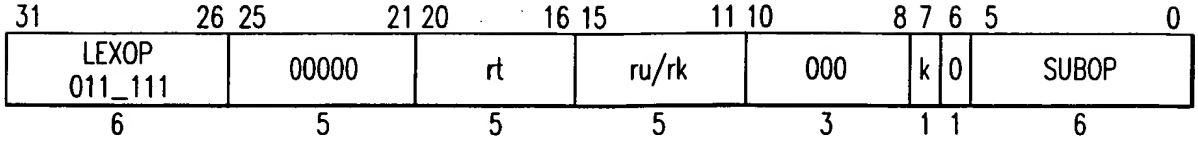
NN=m0-m3
HL
00=RESERVED
01=mN1
10=mNh
11=mN

s

SELECTS SATURATION OF RESULT. s=1 INDICATES THAT SATURATION IS PERFORMED.

FIG.17E

VI. RADIAX MOVE FORMAT AND LEXRA-COP0 MTLXC0/MFLXC0 INSTRUCTIONS



ASSEMBLER MNEMONIC	rt	ru/rk	k	LEXRA SUBOP
MFRU	rt	ru	0	MFRAD
MTRU	rt	ru	0	MTRAD
MFRK	rt	rk	1	MFRAD
MTRK	rt	rk	1	MTRAD

rt

SELECTS GENERAL REGISTER r0-r31.

rk

SELECTS RADIAX KERNEL REGISTER IN MFRK,MTRK INSTRUCTIONS-CURRENTLY ALL RESERVED. HOWEVER, A COPROCESSOR UNUSABLE EXCEPTION IS TAKEN IN USER MODE IF THE Cu0 BIT IS 0 IN THE CP0 STATUS REGISTER WHEN MFRK OR MTRK IS EXECUTED.

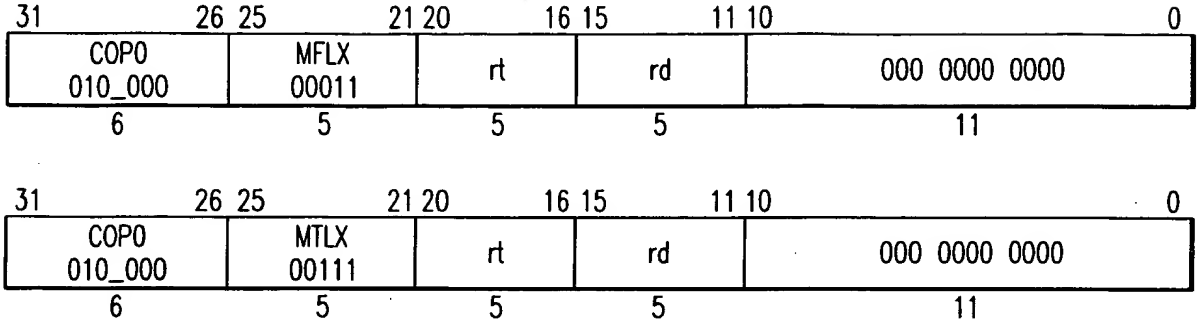
ru

SELECTS RADIAX USER REGISTER IN MFRU,MTRU INSTRUCTIONS.

00000 cbs0
00001 cbs1
00010 cbs2
00011 RESERVED
00100 cbe0
00101 cbe1
00110 cbe2
00111 RESERVED
01xxx RESERVED
10000 lps0
10001 lpe0
10010 lpc0
10011 RESERVED
101xx RESERVED
11000 mmd
11001 RESERVED
111xx RESERVED

FIG.17F

LEXRA-COPROCESSOR0 REGISTER ACCESS INSTRUCTIONS



ASSEMBLER MNEMONIC	Copz rs	rt	rd
MFLXC0	MFLX	rt	rd
MTLXC0	MTLX	rt	rd

THESE ARE NOT LEXOP INSTRUCTIONS. THEY ARE VARIANTS OF THE STANDARD MTC0 AND MFC0 INSTRUCTIONS THAT ALLOW ACCESS TO THE LEXRA COPROCESSOR0 REGISTERS LISTED BELOW. AS WITH ANY COP0 INSTRUCTION, A COPROCESSOR UNUSABLE EXCEPTION IS TAKEN IN USER MODE IF THE Cu0 BIT IS 0 IN THE CP0 STATUS REGISTER WHEN THESE INSTRUCTIONS ARE EXECUTED.

rt

SELECTS GENERAL REGISTER r0-r31.

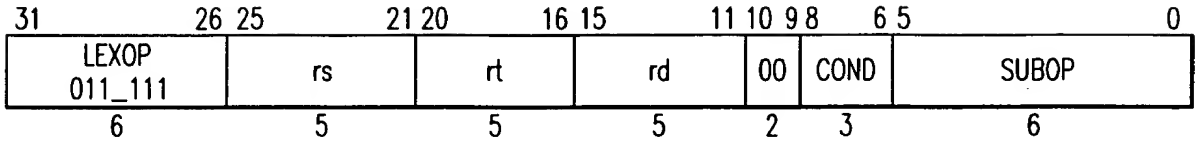
rd

SELECTS LEXRA COPROCESSOR0 REGISTER:

00000 ESTATUS
00001 ECAUSE
00010 INTVEC
00011 RESERVED
001xx RESERVED
01xxx RESERVED
1xxxx RESERVED

FIG.17G

VII. CMOVE FORMAT



ASSEMBLER MNEMONIC	rs	rt	rd	COND	LEXRA SUBOP
CMVEQZ[.H][.L]	rs	rt	rd	COND	CMOVE
CMVNEZ[.H][.L]	rs	rt	rd	COND	CMOVE

rs,rt,rd

SELECTS GENERAL REGISTER r0–r31.

COND

CONDITION CODE FOR rT OPERAND REFERENCED BY THE CONDITIONAL MOVE.

000 EQZ
001 NEZ
010 EQZ.H
011 NEZ.H
100 EQZ.L
101 NEZ.L
11x RESERVED

FIG.17H